UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,713	03/19/2004	John E. Barth Jr.	BUR920030191	2712

29371 7590 11/28/2005

CANTOR COLBURN LLP
55 GRIFFIN ROAD SOUTH
BLOOMFIELD, CT 06002

EXAMINER	
HUR, JUNG H	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/708,713	BARTH ET AL.	
	Examiner	Art Unit	
	Jung (John) Hur	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-7,10-13 and 16-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,6,7,10,12,13,16 and 18* is/are rejected.

7)☒ Claim(s) *5,11 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Amendment

1. Acknowledgment is made of applicant's Amendment, filed 12 September 2005. The changes and remarks disclosed therein have been considered.

Claims 2, 3, 8, 9, 14 and 15 have been cancelled by the Amendment. Therefore, claims 1, 4-7, 10-13 and 16-18 are pending in the application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 4, 6, 7, 10, 12, 13, 16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ackland et al. (U.S. Pat. No. 5,604,705) in view of Wong (U.S. Pat. No. 6,341,083).

Regarding claims 1, 7 and 13, Ackland, for example in Figs. 1 and 2, discloses a method and an apparatus for implementing a read operation for a static random access memory (SRAM) cell (see for example the title and the abstract), the method comprising: activating a word line associated with the SRAM cell (inherent); deactivating a precharge circuit (including T12 and T13) configured for precharging a pair of complementary bit lines (BIT and /BIT) associated with the SRAM cell (see PRE signal at a low state during SENSE and EVAL cycles in Fig. 2);

selectively coupling a corresponding pair of complementary sense amplifier data lines (B and BN) to said pair of complementary bit lines associated with the SRAM cell (by activating T1 and T2; see SELECT signal in Fig. 2); and setting a sense amplifier (including T3-T6) so as to amplify a signal developed on said sense amplifier data lines (by activating T7; see EN signal in Fig. 2), wherein said bit line pair remains coupled to said sense amplifier data lines at the time said sense amplifier is set (see EN signal at a high state and SELECT signal at a high state during EVAL cycle; note that SELECT signal at a high state activates T1 and T2; column 2, lines 40-49).

Ackland does not disclose configuring the SRAM cell with PFET access transistors (or a pair of PFET access transistors associated with the SRAM cell) so as to clamp one of said pair of complementary sense amplifier data lines to a logic high voltage upon activation of a word line associated with the SRAM cell.

Wong, for example in Fig. 2A, discloses a pair of PFET access transistors (PL and PR) associated with an SRAM cell (Fig. 2A) configured to clamp one of a pair of complementary bit lines (BL and BR) to a logic high voltage upon activation of a word line (WL) associated with the SRAM cell (since the bitlines BL and BR would be precharged to VDD and one of complementary nodes CR and CL would be at VDD when the word line WL is activated with a logic low voltage or GND voltage, thus clamping the bitline associated with the logic high voltage node to the logic high voltage through the corresponding pull up transistor P1 or P2; see for example column 5, lines 25-36 and 60-64 and column 6, lines 24-44).

Since Wong teaches that an SRAM cell with PFET access transistors improves the cell stability, lowers the cell power dissipation, and requires less surface area (see for example

column 1, lines 5-11), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to apply the sensing means of Ackland to the SRAM cell of Wong, such that one of the PFET access transistors and one of the pull up transistors within the SRAM cell would also clamp one of the pair of sense amplifier data lines to the logic high voltage (via T1 and T2 in Fig. 1 of Ackland), for the purpose of providing a high speed, less complex, low power means for sensing SRAM cells with PFET access transistors (see for example Ackland column 1, lines 56-62).

Regarding claims 4, 6, 10, 12, 16 and 18, the above Ackland/Wong combination further discloses that said clamping (or said clamp) is implemented through one of a pair of pull up transistors within the SRAM cell (P1 or P2 in Fig. 2A of Wong, providing a path to VDD); wherein said pair of complementary sense amplifier data lines is coupled to said corresponding pair of complementary bit lines through a pair of activated bit switches (T1 and T2 in Fig. 1 of Ackland).

Allowable Subject Matter

4. Claims 5, 11 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The record of the prosecution as a whole makes clear the reasons for the indication of allowable subject matter.

Response to Arguments

5. Applicant's arguments filed 12 September 2005 have been fully considered but they are not persuasive.

In the top paragraph on page 7, Applicant argues that "[b]y not even depicting an exemplary SRAM cell (or the access transistors thereto) in the specification thereof, Ackland thus teaches away from modifying its sense amplifier to have the high-side bitline clamping function provided by an SRAM cell itself since a conventional SRAM cell uses NFET access devices (which do not pass a logic high voltage)."

In response, it is noted that Wong teaches other advantages and benefits of using PFET access transistors (see for example Wong column 3, lines 40-65) in place of NFET access transistors of a conventional SRAM cell, which would motivate one of ordinary skill in the art to use Wong's SRAM cell, instead of the conventional SRAM cell, with the sensing means of Ackland, to obtain the advantages and benefits of both.

In the middle paragraph on page 7, Applicant argues that "[i]n one respect, the Wong reference, by itself, provides no motivation to use its PFET access transistors or cell pull-up devices as clamps to maintain one of the bitline voltages at a high voltage level, since Wong does not provide any details of the operation of sense amplifier circuitry whatsoever."

In response, it is noted that Wong teaches, in using PFET access transistors as disclosed, the advantages of minimizing the size of the transistors with no degradation of the cell stability, guaranteeing an electrical conductivity ratio of 2 (which is related to the cell stability) even though the physical channel size ratio is reduced to 1, and significantly improving cell stability

and reducing power dissipation (see for example Wong, column 3, lines 46-55). Therefore, Wong's teaching of improving cell stability by using PFET access transistors as disclosed implies that the PFET access transistors and the PFET pull-up devices would be operated to clamp (or to maintain the state of) the high-side bitline voltage.

In the bottom paragraph on page 7, Applicant argues that "there is still no teaching in Wong that the PFET access transistors of the SRAM cell can also be used to implement a clamping function for maintaining any signal (much less a high-side bitline) to thereby improve the signal development time when reading data from the SRAM cell. On the contrary, since a primary purpose of Wong is to reduce cell area by using smaller PFET devices with respect to conventional NFET devices..., it stands to reason that the internal PFET pull-up devices of the Wong SRAM cell would not be capable of sufficiently clamping a high-side bitline voltage to the logic high value" (emphases added by Applicant), and further argues, on page 8, that "[s]ince Wong strives for cell size reduction, this reference actually teaches away from using the cell access transistor (and hence the using the cell's pull-up transistors as clamping devices) since such an application would necessarily limit the extent to which the pull-up devices can be minimized while also providing sufficient clamping strength" (emphasis added by Applicant).

In response, it is noted that Wong teaches additional purposes for using PFET access transistors as disclosed, including minimizing the size of the transistors with no degradation of the cell stability, guaranteeing an electrical conductivity ratio of 2 (which is related to the cell stability) even though the physical channel size ratio is reduced to 1, and significantly improving cell stability and reducing power dissipation (see for example Wong, column 3, lines 46-55).

Therefore, these additional purposes would motivate one of ordinary skill in the art to combine Wong with Ackland to obtain the benefits and advantages of both. Further, Wong's teaching of improving cell stability by using PFET access transistors as disclosed implies that the PFET access transistors and PFET pull-up devices would be operated to clamp (or to maintain the state of) the high-side bitline voltage.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (571) 272-1870. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jhh

VAN THU NGUYEN
PRIMARY EXAMINER